Listing of Claims

Claim 1 (Currently Amended): The method of claim 9, wherein said communication path has ~~A method of sharing~~ a line bandwidth ~~on a communication path among a plurality of virtual circuits in an ATM Device~~, said line bandwidth equaling a line rate, wherein said plurality of virtual circuits comprise a plurality of VC-types, said method further comprising:

accepting a configuration of said plurality of virtual circuits, wherein a sum of allocated bandwidths of said plurality of virtual circuits exceeds said line rate;

~~receiving a plurality of cells on said plurality of virtual circuits; and~~

scheduling for transmission said plurality of cells on said communication path while enforcing a pre-specified priority with respect to said plurality of VC-types and while limiting bandwidth usage by each of said plurality of virtual circuits to a corresponding allocated bandwidth.

Claim 2 (Original): The method of claim 1, wherein said plurality of VC-types comprise constant bit rate (CBR) VC-type, variable bit rate-real time (VBR-RT) VC-type, variable bit rate - non real time (VBR-nRT) VC-type, wherein said pre-specified priority comprises highest to lowest priority for CBR VC-type, VBR-RT VC-type and VBR-nRT VC-type in that order, wherein a first cell related to a lower priority VC-type is scheduled for transmission only if no cells of a higher priority VC-type are ready for transmission.

Claim 3 (Original): The method of claim 2, wherein said plurality of VC-types further comprises unspecified bit rate (UBR) VC-type, wherein UBR VC-type is given lower priority than said VBR-nRT VC-type.

Claim 4 (Original): The method of claim 2, wherein said scheduling comprises:

determining cell slots in which of each of said plurality of virtual circuits is a candidate for allocation according to a corresponding allocated bandwidth, wherein a first virtual circuit of a first VC-type and a second virtual circuit of a second VC-type are determined to be candidates for allocation in a first cell slot on said communication path, wherein said first VC-type is different from said second VC-type; and

allocating said first cell slot to one of said first virtual circuit and said second virtual circuit having a higher priority if the virtual circuit with the higher priority has a cell ready for transmission.

Claim 5 (Original): The method of claim 4, wherein said scheduling further comprises allocating said first cell slot to one of said first virtual circuit and said second virtual circuit having a lower priority if the virtual circuit with the higher priority does not have a cell ready for transmission and if the virtual circuit with the lower priority has a cell ready for transmission.

Claim 6 (Canceled)

Claim 7 (Currently Amended): A method of determining the specific cell to transmit in each of a sequence of successive slots on a communication path coupled to an ATM switch, said method being performed in said ATM switch, said method comprising: ~~The method of claim 6, wherein said maintaining comprises:~~

receiving a plurality of sequences of cells, each sequence of cells being received on a corresponding one of a plurality of virtual circuits (VCs), each virtual circuit having an associated allocated bandwidth;

initializing ~~said~~ a VC-credit counter and a line slot credit counter associated with ~~said~~ each of said plurality of virtual circuits including a fourth virtual circuit to zero;

computing an inter-cell delay associated with each of said plurality of virtual circuits including said fourth virtual circuit, wherein the inter-cell delay is computed to have a negative correlation to the magnitude of ~~according to~~ the corresponding allocated bandwidth; ~~and~~

incrementing said line slot credit counter by a token value in each cell slot of said communication path, wherein said token value is determined by a length of duration of cell slots on said communication path;

incrementing said VC-credit counter of each virtual circuit by one if said line slot credit counter of the corresponding virtual circuit is equal to or greater than said inter-cell delay and if said VC-credit counter is already not equal to a ~~said~~ maximum number specified by corresponding virtual circuit;

scheduling a cell of said fourth virtual circuit for transmission in a slot only if said VC credit counter is greater than or equal to 1 for that slot;

decrementing said line slot credit counter by said inter-cell delay when said VC-credit counter is incremented; and

decrementing said VC-credit counter by one when a cell related to said fourth virtual circuit is scheduled for transmission.

Claim 8 (Currently Amended): The method of claim 7, further comprising:

computing a peak maximum slot credit and a peak intercell delay associated with ~~a fifth~~ said fourth virtual circuit if said fourth virtual circuit is of a type having a peak cell rate (PCR) in addition to allocated bandwidth, wherein said peak intercell delay and said peak maximum slot credit are computed ~~according to a corresponding peak cell rate (PCR)~~ to have a negative correlation with a magnitude of said PCR;

initializing a peak slot credit associated with said ~~fifth~~ fourth virtual circuit to zero;

incrementing said peak slot credit by said token value in each cell slot, but said peak slot credit being capped at said peak maximum slot credit;

decrementing said peak slot credit by said peak intercell delay if a cell associated with said ~~fifth~~ fourth virtual circuit is scheduled for transmission; and

scheduling for transmission a cell on said ~~fifth~~ fourth virtual circuit only if said peak slot credit is greater than or equal to said peak intercell delay.

Claim 9 (Currently Amended): The method of claim 8, ~~wherein said fourth virtual circuit is of CBR VC-type, and~~ wherein said maximum number equals 1 if said fourth virtual circuit is of CBR VC-type and greater than 1 in case of VBR-type.

Claim 10 (Currently Amended): The method of claim 8, wherein said fourth virtual circuit is ~~the same as said fifth virtual circuit and is~~ of VBR VC-type, and wherein said maximum number is computed according to the equation [MBS - (MBS x SCR/PCR) - 1], wherein - and x respectively represent a subtraction and a multiplication operation, PCR

represents peak cell rate, SCR represents sustained cell rate, and MBS represents maximum burst size of said fourth virtual circuit.

Claim 11 (Original): The method of claim 8, wherein said ATM device comprises one of a CPE, an ATM switch and a edge router.

Claim 12 (Currently Amended): ~~A~~ The machine readable medium of claim 18, wherein said communication path has ~~A method of sharing~~ a line bandwidth ~~on a communication path among a plurality of virtual circuits in an ATM Device, carrying one or more sequences of instructions for causing an ATM device to share a line bandwidth on a communication path among a plurality of virtual circuits~~, said line bandwidth equaling a line rate, wherein said plurality of virtual circuits comprise a plurality of VC-types~~, wherein execution of said one or more sequences of instructions by one or more processors contained in said ATM device causes said one or more processors to perform the actions of~~ further comprising:

accepting a configuration of said plurality of virtual circuits, wherein a sum of allocated bandwidths of said plurality of virtual circuits exceeds said line rate;

~~receiving a plurality of cells on said plurality of virtual circuits;~~ and

scheduling for transmission said plurality of cells on said communication path while enforcing a pre-specified priority with respect to said plurality of VC-types and while limiting bandwidth usage by each of said plurality of virtual circuits to a corresponding allocated bandwidth.

Claim 13 (Original): The machine readable medium of claim 12, wherein said plurality of VC-types comprise constant bit rate (CBR) VC-type, variable bit rate-real time (VBR-RT) VC-type, variable bit rate - non real time (VBR-nRT) VC-type, wherein said pre-specified priority comprises highest to lowest priority for CBR VC-type, VBR-RT VC-type and VBR-nRT VC-type in that order, wherein a first cell related to a lower priority VC-type is scheduled for transmission only if no cells of a higher priority VC-type are ready for transmission.

Claim 14 (Original): The machine readable medium of claim 13, wherein said plurality of VC-types further comprises unspecified bit rate (UBR) VC-type, wherein UBR VC-type is given lower priority than said VBR-nRT VC-type.

Claim 15 (Original): The machine readable medium of claim 13, wherein said scheduling comprises:

determining cell slots in which of each of said plurality of virtual circuits is a candidate for allocation according to a corresponding allocated bandwidth, wherein a first virtual circuit of a first VC-type and a second virtual circuit of a second VC-type are determined to be candidates for allocation in a first cell slot on said communication path, wherein said first VC-type is different from said second VC-type; and

allocating said first cell slot to one of said first virtual circuit and said second virtual circuit having a higher priority if the virtual circuit with the higher priority has a cell ready for transmission.

Claim 16 (Original): The machine readable medium of claim 15, wherein said scheduling further comprises allocating said first cell slot to one of said first virtual circuit and said second virtual circuit having a lower priority if the virtual circuit with the higher priority does not have a cell ready for transmission and if the virtual circuit with the lower priority has a cell ready for transmission.

Claim 17 (Canceled)

Claim 18 (Currently Amended): A machine readable medium carrying one or more sequences of instructions for causing an ATM device to determine the specific cell to transmit in each of a sequence of successive slots on a communication path coupled to said ATM switch, wherein execution of said one or more sequences of instructions by one or more processors contained in said ATM device causes said one or more processors to perform the actions of:

~~The machine readable medium of claim 17, wherein said maintaining comprises:~~

receiving a plurality of sequences of cells, each sequence of cells being received on a corresponding one of a plurality of virtual circuits (VCs), each virtual circuit having an associated allocated bandwidth;

initializing ~~said~~ a VC-credit counter and a line slot credit counter associated with ~~said~~ each of said plurality of virtual circuits including a fourth virtual circuit to zero;

computing an inter-cell delay associated with each of said plurality of virtual circuits including said fourth virtual circuit, wherein the inter-cell delay is computed to have a

negative correlation to the magnitude of ~~according to~~ the corresponding allocated bandwidth; ~~and~~

incrementing said line slot credit counter by a token value in each cell slot of said communication path, wherein said token value is determined by a length of duration of cell slots on said communication path;

incrementing said VC-credit counter of each virtual circuit by one if said line slot credit counter of the corresponding virtual circuit is equal to or greater than said inter-cell delay and if said VC-credit counter is already not equal to a ~~said~~ maximum number specified by corresponding virtual circuit;

scheduling a cell of said fourth virtual circuit for transmission in a slot only if said VC credit counter is greater than or equal to 1 for that slot;

decrementing said line slot credit counter by said inter-cell delay when said VC-credit counter is incremented; and

decrementing said VC-credit counter by one when a cell related to said fourth virtual circuit is scheduled for transmission.

Claim 19 (Currently Amended): The machine readable medium of claim 18, further comprising:

computing a peak maximum slot credit and a peak intercell delay associated with ~~a fifth~~ said fourth virtual circuit if said fourth virtual circuit is of a type having a peak cell rate (PCR) in addition to allocated bandwidth, wherein said peak intercell delay and said peak maximum slot credit are computed ~~according to a corresponding peak cell rate (PCR)~~ to have a negative correlation with a magnitude of said PCR;

initializing a peak slot credit associated with said ~~fifth~~ fourth virtual circuit to zero;

incrementing said peak slot credit by said token value in each cell slot, but said peak slot credit being capped at said peak maximum slot credit;

decrementing said peak slot credit by said peak intercell delay if a cell associated with said ~~fifth~~ fourth virtual circuit is scheduled for transmission; and

scheduling for transmission a cell on said fifth virtual circuit only if said peak slot credit is greater than or equal to said peak intercell delay.

Claim 20 (Currently Amended): The machine readable medium of claim 19, ~~wherein said fourth virtual circuit is of CBR VC-type, and~~ wherein said maximum number equals 1 if said fourth virtual circuit is of CBR VC-type and greater than 1 in case of VBR-type.

Claim 21 (Original): The machine readable medium of claim 19, wherein said fourth virtual circuit is ~~the same as said fifth virtual circuit and is~~ of VBR VC-type, and wherein said maximum number is computed according to the equation [MBS - (MBS x SCR/PCR) - 1], wherein - and x respectively represent a subtraction and a multiplication operation, PCR represents peak cell rate, SCR represents sustained cell rate, and MBS represents maximum burst size of said fourth virtual circuit.

Claim 22 (Original): The machine readable medium of claim 19, wherein said ATM device comprises one of a CPE, an ATM switch and a edge router.

Claim 23 (Currently Amended): ~~An~~ The ATM device of claim 29, wherein said communication path has ~~sharing~~ a line bandwidth ~~on a communication path among a plurality of virtual circuits~~, said line bandwidth equaling a line rate, wherein said plurality of virtual circuits comprise a plurality of VC-types, said ATM device further comprising:

means for accepting a configuration of said plurality of virtual circuits, wherein a sum of allocated bandwidths of said plurality of virtual circuits exceeds said line rate;

~~means for receiving a plurality of cells on said plurality of virtual circuits;~~ and

means for scheduling for transmission said plurality of cells on said communication path while enforcing a pre-specified priority with respect to said plurality of VC-types and while limiting bandwidth usage by each of said plurality of virtual circuits to a corresponding allocated bandwidth.

Claim 24 (Original): The ATM device of claim 23, wherein said plurality of VC-types comprise constant bit rate (CBR) VC-type, variable bit rate-real time (VBR-RT) VC-type, variable bit rate - non real time (VBR-nRT) VC-type, wherein said pre-specified priority comprises highest to lowest priority for CBR VC-type, VBR-RT VC-type and VBR-nRT VC-type in that order, wherein a first cell related to a lower priority VC-type is scheduled for transmission only if no cells of a higher priority VC-type are ready for transmission.

Claim 25 (Original): The ATM device of claim 24, wherein said plurality of VC-types further comprises unspecified bit rate (UBR) VC-type, wherein UBR VC-type is given lower priority than said VBR-nRT VC-type.

Claim 26 (Original): The ATM device of claim 24, wherein said means for scheduling is operable to:

determine cell slots in which of each of said plurality of virtual circuits is a candidate for allocation according to a corresponding allocated bandwidth, wherein a first virtual circuit of a first VC-type and a second virtual circuit of a second VC-type are determined to be candidates for allocation in a first cell slot on said communication path, wherein said first VC-type is different from said second VC-type; and

allocate said first cell slot to one of said first virtual circuit and said second virtual circuit having a higher priority if the virtual circuit with the higher priority has a cell ready for transmission.

Claim 27 (Original): The ATM device of claim 26, wherein said means for scheduling is further operable to allocate said first cell slot to one of said first virtual circuit and said second virtual circuit having a lower priority if the virtual circuit with the higher priority does not have a cell ready for transmission and if the virtual circuit with the lower priority has a cell ready for transmission.

Claim 28 (Canceled)

Claim 29 (Currently Amended): ~~The~~ An ATM device to transmit cells in a sequence of successive slots on a communication path, said ATM device comprising: ~~of claim 28, wherein said means for maintaining is operable to:~~

means for receiving a plurality of sequences of cells, each sequence of cells being received on a corresponding one of a plurality of virtual circuits (VCs), each virtual circuit having an associated allocated bandwidth;

means for initializing ~~initialize said~~ a VC-credit counter and a line slot credit counter associated with ~~said~~ each of said plurality of virtual circuits including a fourth virtual circuit to zero;

means of computing an inter-cell delay associated with each of said plurality of virtual circuits including said fourth virtual circuit, wherein the inter-cell delay is computed to have a negative correlation to the magnitude of ~~according to~~ the corresponding allocated bandwidth; ~~and~~

means for incrementing said line slot credit counter by a token value in each cell slot of said communication path, wherein said token value is determined by a length of duration of cell slots on said communication path;

means for incrementing said VC-credit counter of each virtual circuit by one if said line slot credit counter of the corresponding virtual circuit is equal to or greater than said inter-cell delay and if said VC-credit counter is already not equal to a ~~said~~ maximum number specified by corresponding virtual circuit;

means for scheduling a cell of said fourth virtual circuit for transmission in a slot only if said VC credit counter is greater than or equal to 1 for that slot;

means for decrementing said line slot credit counter by said inter-cell delay when said VC-credit counter is incremented; and

means for decrementing said VC-credit counter by one when a cell related to said fourth virtual circuit is scheduled for transmission.

Claim 30 (Currently Amended): The ATM device of claim 29, ~~wherein said means for maintaining is operable to~~ further comprising:

means for computing a peak maximum slot credit and a peak intercell delay associated with ~~a fifth~~ said fourth virtual circuit if said fourth virtual circuit is of a type having a peak cell rate (PCR) in addition to allocated bandwidth, wherein said peak intercell delay and said peak maximum slot credit are computed ~~according to a corresponding peak cell rate (PCR)~~ to have a negative correlation with a magnitude of said PCR;

means for initializing a peak slot credit associated with said ~~fifth~~ fourth virtual circuit to zero;

means for incrementing said peak slot credit by said token value in each cell slot, but said peak slot credit being capped at said peak maximum slot credit;

means for decrementing said peak slot credit by said peak intercell delay if a cell associated with said ~~fifth~~ fourth virtual circuit is scheduled for transmission; and

means for scheduling for transmission a cell on said ~~fifth~~ fourth virtual circuit only if said peak slot credit is greater than or equal to said peak intercell delay.

Claim 31 (Currently Amended): The ATM device of claim 30, ~~wherein said fourth virtual circuit is of CBR VC-type, and~~ wherein said maximum number equals 1 if said fourth virtual circuit is of CBR VC-type and greater than 1 in case of VBR-type.

Claim 32 (Currently Amended): The ATM device of claim 30, wherein said fourth virtual circuit is ~~the same as said fifth virtual circuit and is~~ of VBR VC-type, and wherein said maximum number is computed according to the equation [MBS - (MBS x SCR/PCR)

- 1], wherein - and x respectively represent a subtraction and a multiplication operation, PCR represents peak cell rate, SCR represents sustained cell rate, and MBS represents maximum burst size of said fourth virtual circuit.

Claim 33 (Original): The ATM device of claim 30, wherein said ATM device comprises one of a CPE, a DSLAM, an ATM switch and a edge router.

Claim 34 (Currently Amended): The ATM device of claim 40, wherein said communication path has ~~sharing~~ a line bandwidth ~~on a communication path among a plurality of virtual circuits~~, said line bandwidth equaling a line rate, wherein said plurality of virtual circuits comprise a plurality of VC-types, said ATM device further comprising:

a memory storing data representing a configuration of said plurality of virtual circuits, wherein a sum of allocated bandwidths of said plurality of virtual circuits exceeds said line rate;

~~an inbound interface receiving a plurality of cells on said plurality of virtual circuits;~~ and

a scheduler block scheduling for transmission said plurality of cells on said communication path while enforcing a pre-specified priority with respect to said plurality of VC-types and while limiting bandwidth usage by each of said plurality of virtual circuits to a corresponding allocated bandwidth.

Claim 35 (Original): The ATM device of claim 34, wherein said plurality of VC-types comprise constant bit rate (CBR) VC-type, variable bit rate-real time (VBR-RT) VC-type,

variable bit rate - non real time (VBR-nRT) VC-type, wherein said pre-specified priority comprises highest to lowest priority for CBR VC-type, VBR-RT VC-type and VBR-nRT VC-type in that order, wherein a first cell related to a lower priority VC-type is scheduled for transmission only if no cells of a higher priority VC-type are ready for transmission.

Claim 36 (Original): The ATM device of claim 35, wherein said plurality of VC-types further comprises unspecified bit rate (UBR) VC-type, wherein UBR VC-type is given lower priority than said VBR-nRT VC-type.

Claim 37 (Original): The ATM device of claim 35, wherein said scheduler block is operable to:

determine cell slots in which of each of said plurality of virtual circuits is a candidate for allocation according to a corresponding allocated bandwidth, wherein a first virtual circuit of a first VC-type and a second virtual circuit of a second VC-type are determined to be candidates for allocation in a first cell slot on said communication path, wherein said first VC-type is different from said second VC-type; and

allocate said first cell slot to one of said first virtual circuit and said second virtual circuit having a higher priority if the virtual circuit with the higher priority has a cell ready for transmission.

Claim 38 (Original): The ATM device of claim 37, wherein said scheduler block is further operable to allocate said first cell slot to one of said first virtual circuit and said second virtual circuit having a lower priority if the virtual circuit with the higher priority does

not have a cell ready for transmission and if the virtual circuit with the lower priority has a cell ready for transmission.

Claim 39 (Canceled)

Claim 40 (Currently Amended): ~~The~~ An ATM device to transmit cells in a sequence of successive slots on a communication path, said ATM device comprising: ~~of claim 39, wherein to maintain said VC-credit, said scheduler block is operable to:~~

an input interface to receive a plurality of sequences of cells, each sequence of cells being received on a corresponding one of a plurality of virtual circuits (VCs), each virtual circuit having an associated allocated bandwidth; and

a scheduler block operable to:

initialize ~~said~~ a VC-credit counter and a line slot credit counter associated with ~~said~~ each of said plurality of virtual circuits including a fourth virtual circuit to zero;

compute an inter-cell delay associated with each of said plurality of virtual circuits including said fourth virtual circuit, wherein the inter-cell delay is computed to have a negative correlation to the magnitude of ~~according to~~ the corresponding allocated bandwidth; ~~and~~

increment said line slot credit counter by a token value in each cell slot of said communication path, wherein said token value is determined by a length of duration of cell slots on said communication path;

increment said VC-credit counter of each virtual circuit by one if said line slot credit counter of the corresponding virtual circuit is equal to or greater than said

inter-cell delay and if said VC-credit counter is already not equal to a ~~said~~ maximum number specified by corresponding virtual circuit;

schedule a cell of said fourth virtual circuit for transmission in a slot only if said VC credit counter is greater than or equal to 1 for that slot;

decrement said line slot credit counter by said inter-cell delay when said VC-credit counter is incremented; and

decrement said VC-credit counter by one when a cell related to said fourth virtual circuit is scheduled for transmission.

Claim 41 (Currently Amended): The ATM device of claim 40, wherein said scheduler block is further operable to:

compute a peak maximum slot credit and a peak intercell delay associated with ~~a fifth~~ said fourth virtual circuit if said fourth virtual circuit is of a type having a peak cell rate (PCR) in addition to allocated bandwidth, wherein said peak intercell delay and said peak maximum slot credit are computed ~~according to a corresponding peak cell rate (PCR)~~ to have a negative correlation with a magnitude of said PCR;

initialize a peak slot credit associated with said ~~fifth~~ fourth virtual circuit to zero;

increment said peak slot credit by said token value in each cell slot, but said peak slot credit being capped at said peak maximum slot credit;

decrement said peak slot credit by said peak intercell delay if a cell associated with said ~~fifth~~ fourth virtual circuit is scheduled for transmission; and

schedule for transmission a cell on said ~~fifth~~ fourth virtual circuit only if said peak slot credit is greater than or equal to said peak intercell delay.

Claim 42 (Currently Amended): The ATM device of claim 41, ~~wherein said fourth virtual circuit is of CBR VC-type, and~~ wherein said maximum number equals 1 if said fourth virtual circuit is of CBR VC-type and greater than 1 in case of VBR-type.

Claim 43 (Currently Amended): The ATM device of claim 41, wherein said fourth virtual circuit is ~~the same as said fifth virtual circuit and is~~ of VBR VC-type, and wherein said maximum number is computed according to the equation [MBS - (MBS x SCR/PCR) - 1], wherein - and x respectively represent a subtraction and a multiplication operation, PCR represents peak cell rate, SCR represents sustained cell rate, and MBS represents maximum burst size of said fourth virtual circuit.

Claim 44 (Original): The ATM device of claim 41, wherein said ATM device comprises one of a CPE, a DSLAM, an ATM switch and a edge router.

Claim 45 (Original): The ATM device of claim 41, wherein said fifth virtual circuit is of UBR type.

Claim 46 (New): The method of claim 7, wherein said VC-credit counter for said fourth virtual circuit is incremented if said VC credit counter is greater than or equal to 1 for that slot even when at least one of a first condition and a second condition is true, wherein said first situation is in which a cell is not available on said fourth virtual circuit for transmission and said second situation is in which a cell on said fourth virtual circuit is

available for transmission but not scheduled for transmission because a cell corresponding to some other eligible virtual circuit is transmitted.

Claim 47 (New): The computer readable medium of claim 12, wherein said VC-credit counter for said fourth virtual circuit is incremented if said VC credit counter is greater than or equal to 1 for that slot even when at least one of a first condition and a second condition is true, wherein said first situation is in which a cell is not available on said fourth virtual circuit for transmission and said second situation is in which a cell on said fourth virtual circuit is available for transmission but not scheduled for transmission because a cell corresponding to some other eligible virtual circuit is transmitted.

Claim 48 (New): The ATM device of claim 29, wherein said VC-credit counter for said fourth virtual circuit is incremented if said VC credit counter is greater than or equal to 1 for that slot even when at least one of a first condition and a second condition is true, wherein said first situation is in which a cell is not available on said fourth virtual circuit for transmission and said second situation is in which a cell on said fourth virtual circuit is available for transmission but not scheduled for transmission because a cell corresponding to some other eligible virtual circuit is transmitted.

Claim 49 (New): The ATM device of claim 40, wherein said VC-credit counter for said fourth virtual circuit is incremented if said VC credit counter is greater than or equal to 1 for that slot even when at least one of a first condition and a second condition is true, wherein said first situation is in which a cell is not available on said fourth virtual circuit for

transmission and said second situation is in which a cell on said fourth virtual circuit is available for transmission but not scheduled for transmission because a cell corresponding to some other eligible virtual circuit is transmitted.